

Appl. No. 10/691,173
Examiner: TRAN, MAI HUONG C, Art Unit 2818
In response to the Office Action dated March 8, 2005

Date: June 8, 2005
Attorney Docket No. 10113081

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A memory device with vertical transistors and trench capacitors, comprising:

- a substrate, having at least one deep trench therein;
- a trench capacitor, deposited in a lower position of the deep trench;
- a conducting structure, deposited on the trench capacitor, comprising a first conductive layer and a second conductive layer;
- a ring shaped insulator, deposited on parts of the sidewall of the deep trench and between the substrate of the deep trench and the first conductive layer, such that the first conductive is surrounded by the ring shaped insulator, wherein the second conductive layer is deposited on the first conductive and the ring shaped insulator;
- a diffusion barrier, deposited on one side of the sidewall of the deep trench and between the second conductive layer and the substrate of the deep trench, comprising a thermal oxide;
- a trench top isolation, deposited on the conducting structure; and
- a control gate, deposited on the trench top isolation.

Claim 2 (original): The memory device as claimed in claim 1, further comprising:

- a buried strap, deposited within the substrate beside parts of the conducting structure where the diffusion barrier is not deposited, serving as a source.

Claim 3 (original): The memory device as claimed in claim 1, further comprising:

- a doping area, provided within the substrate beside the control gate, serving as a drain.

Claim 4 (original): The memory device as claimed in claim 1, wherein the ring shaped insulator comprises an oxide.

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Claim 5 (original): The memory device as claimed in claim 1, wherein the first conductive layer comprises a doped polysilicon or a doped amorphous silicon.

Claim 6 (original): The memory device as claimed in claim 1, wherein the second conductive layer comprises a doped polysilicon or a doped amorphous silicon.

Claim 7 (canceled)

Claim 8 (original): The memory device as claimed in claim 1, wherein the thickness of the diffusion barrier is substantially less than 100Å.

Claim 9 (original): The memory device as claimed in claim 1, wherein the trench top isolation comprises an oxide.

Claim 10 (original): The memory device as claimed in claim 1, wherein the control gate comprises a gate layer and a gate dielectric layer deposited between the gate layer and the substrate.

Claim 11 (original): The memory device as claimed in claim 1, wherein the gate layer comprises a polysilicon, a silicide, a metal layer, or a combination thereof.

Claim 12 (original): The memory device as claimed in claim 1, wherein the gate dielectric layer comprises an oxide.

Claim 13 (original): The memory device as claimed in claim 2, wherein the buried strap is electrically connected with the control gate and formed by diffusing dopants of the first conductive layer into the substrate of the trench surrounding the top of the second conductive layer.

Claims 14-42 (canceled)